AREA EFFICIENT AND FAULT TOLERANT FIR FILTER

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Abstract— Triple Modular Redundancy (TMR) and Hamming Codes have been used to protect different circuits against Single Event Upsets (SEUs). In this paper, the use of a Novel Hamming approach on FIR Filters is studied and implemented in order to provide low complexity , reduce delay and area efficient protection techniques for higher bits data.

Index Terms— Single Event Upset (SEU), Hamming codes, Novel Hamming codes, Reliability, Digital filters, FPGA, Xilinx 9.2

1. INTRODUCTION

Memory cells have been protected from soft errors for more than a decade; due to the increase in soft error rate in logic circuits, the encoder and decoder circuitry around the memory blocks have become susceptible to soft errors as well and must also be protected

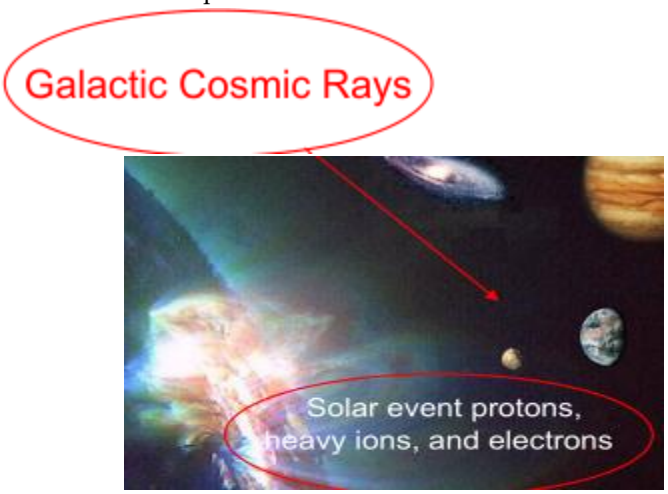

Figure 1 : Energetic particles causing SEEs

In some environments, such as space, radiation sources are abundant as is evident in figure 1 . The effects of radiations are a well-known cause of errors in microelectronic circuits [1]. These errors range from temporary failures of the system (which most of the times produce a restart of the operations) to serious and permanent damage of the devices. One type of temporary effects is Single Event Effects (SEEs), that cause undesirable changes in the values of flips -flops (SEUs) or combinational logic (SETs) [2]. When a particle hits the silicon, it loses its energy and transmits it to the silicon, causing a current burst. In the case of SEUs, these can randomly change the content of storage cells. To protect storage cells of integrated circuits from this phenomenon, several approaches may be followed[3][4]. One is by technology hardening of memory cells and another one is by designing circuits able to detect an SEU event and act accordingly to prevent error propagation and guarantee full reliability in the system. Triple Modular Redundancy (TMR) and Error Detection and Correction Code (EDAC), like Hamming Code, are examples of such methods.

Filters are commonly used in digital communication systems for equalization, signal separation, noise reduction, etc. As communications are fundamental for space borne applications, such as satellites, unmanned missions, etc., digital filters play an important role in space systems [5].

This paper introduces optimizations for the use of improved Hamming Codes to protect generic (FIR) filter, described by (1) and illustrated in Figure 2. It shows that by knowing attributes of the design to protect the circuit, it is possible to reduce resource consumption and achieve an optimal design.

$$\sum_{i=0}^{N-1} x[n-i].h[i] \quad \text{.....(1)}$$

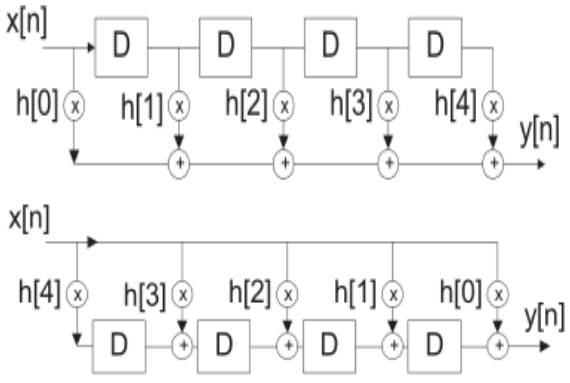

Figure 2 : Direct Form FIR filter structure and transposed FIR Filter structure.

HAMMING code is well known for its single-bit error detection and correction capability. Hamming code is based on the principle of adding 'r' redundancy bits to 'n' data bits such that

$$2^r \geq n + r + 1$$

For example, it needs 4 redundancy bits for a 7-bit data item and 6 redundancy bits for a 56-bit data stream. Let us say, the 7-bit data to be transmitted is 0111001. Then the 11-bit data actually transmitted is 011P100P1PP, where the P's refer to the Hamming bits that are to be calculated and interspersed at bit positions 1, 2, 4, & 8. Thus the 11-bit data actually transmitted is 011**0**100**1**1**1**. For the calculation of Hamming bits at positions 1, 2, 4, & 8, even-parity checks were performed on 6, 6, 4, & 4 bits respectively. Thus a total of 20 bits are involved in the process of Hamming bits calculations. The error-detection and correction process in Hamming code is as illustrated in Table 1 Hamming code is normally used for transmission of 7-bit data item. Scaling it for larger data lengths results in a lot of overhead due to interspersing the redundancy bits and their removal later, it is not efficient for higher data bit

2. PROPOSED NOVEL HAMMING CODE

A novel Hamming code is proposed in this section , to increase the efficiency of higher data bits. Let us consider the same example. The 7-bit data to be transmitted is 0111001. The number of redundancy bits, 'r' to be appended to n-bit data is obtained such that the relation

$$(2^{r-1} - 1) \geq n$$

is satisfied. The number of redundancy bits in this method is same as that for Hamming code for some values of n. But in some cases, it will be just one more redundancy bit than needed in the Hamming code[6][7][8]. For 7-bit data, the number of redundancy bits required will be 4. Then the 11-bit data actually transmitted is PPPP0111001, where the P's refer to the redundancy bits that are to be calculated and appended at bit positions 8, 9, 10, & 11. Thus the 11-bit data actually transmitted is **0110**0111001. For the calculation of bits at positions 8, 9, 10, & 11, even-parity checks were performed on 5, 5, 5, & 4 bits respectively. Thus a total of 19 bits are involved in the process of calculation of redundancy bits. The error-detection and correction process as proposed in this novel method is illustrated in Table 2.

TABLE1 : ERROR DETECTION AND CORRECTION USING HAMMING CODE

Recieved information include Hamming bits											Status of Parity check				Conclusion
11	10	9	8	7	6	5	4	3	2	1	S3	S2	S1	S0	
0	1	1	0	1	0	**1**	1	1	1	1	T	F	T	F	Error at bit position 5
0	1	1	**1**	1	0	0	1	1	1	1	F	T	T	T	Error at bit position 8
0	1	1	0	1	0	0	1	1	1	1	T	T	T	T	No Error

TABLE 2 : ERROR DETECTION AND CORRECTION USING NOVEL METHOD

Recieved information including redundancy bits											Status of Parity check				Conclusion
11	10	9	8	7	6	5	4	3	2	1	S3	S2	S1	S0	
0	1	1	0	0	**0**	1	1	0	0	1	T	F	F	T	Error at bit position 6
0	1	1	**1**	0	1	1	1	0	0	1	F	T	T	F	Error at bit position 8
0	1	**0**	0	0	1	1	1	0	0	1	F	T	F	T	Error at bit position 9
0	**0**	1	0	0	1	1	1	0	0	1	F	F	T	T	Error at bit position10
1	1	1	0	0	1	1	1	0	0	1	T	F	T	T	Error at bit position11
0	1	1	0	0	1	1	1	0	0	1	T	F	T	T	No Error

TABLE 3 : COMPARISON OF NUMBER OF BITS INVOLVED IN CALCULATION OF REDUNDANCY BITS

Length of data stream	Number of bits involved in calculation of Redundancy bits in **Hamming code**	Number of bits involved in calculation of Redundancy bits in **Novel Hamming code**
7 bit data	20 bits involved	19 bits involved
31 bit data	93 bits involved	90 bits involved
56 bit data	182 bits involved	172 bits involved

TMR is the simplest and effective way for protecting a design. The area consumption of this method is obviously up to three times higher, depending on which implementation is chosen. The optimal design of the TMR logic is discussed in [9]. A previous approach to protect FIR filters using Hamming codes as discussed in [10] is illustrated in Fig. 3 and Fig. 4. EDAC codes to protect the circuit incurs a great achievement in terms of area with respect to the use of TMR [10]

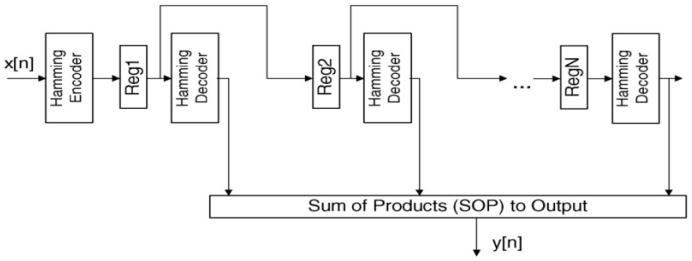

FIGURE 3 : FIR filter protection with a single encoder

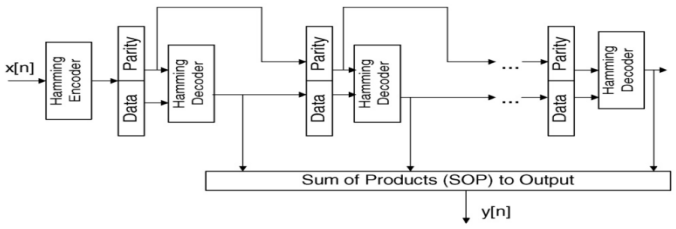

FIGURE 4 : FIR filter protection with additional data protection

3 . IMPLEMENTATION OF PROPOSED TECHNIQUE

In this section, the proposed technique is used to demonstrate, how the lot of overhead due to interspersing the redundancy bits , their subsequent removal, pad to pad delay in the decoder and consumption of total area of FIR filter for higher bits are reduced. These are based on the novel hamming code implementation in the FIR filter instead of conventional hamming code used to protect FIR filter previously[10].

A . Novel Hamming Single Encoder

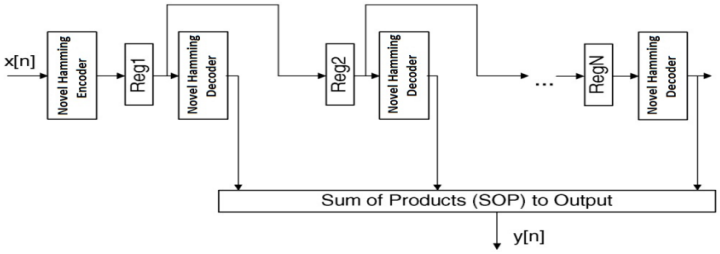

FIGURE 5 : FIR filter protection with a single Novel encoder

One of the improvisation would be to replace the Hamming encoders and Hamming decoder[10] with Novel Hamming encoder and Novel Hamming decoder respectively, in Fig. 3. The delay in the Novel Hamming decoder reduced in comparison of conventional Hamming decoder, they are only used if there are errors in the circuit and even in that case, if only a single error is present in the register, it can still be corrected with the Novel decoder at each stage. In summary, these additional encoders are useful only if we assume that a tap value will be hit by more than one SEU at different time instants, as it propagates through the delay line

B. Novel Additional Hamming Data Protection

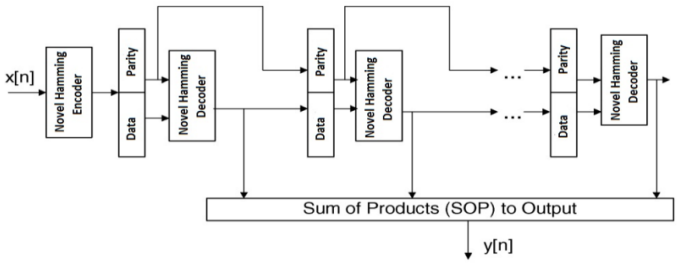

FIGURE 6 : FIR filter protection with Novel additional data protection

The operation observed in the above design (fig. 5) is improved in this section by using a novel addition Hamming data protection. Here , the output of each decoder is fed to the data bits of the next register while the parity bits are taken directly from the previous stage, as shown in Figure 6. This would allow recovering from multiple errors that occur in the data bits as long as they happen in different clock cycles. This is achieved without additional encoders.

4. EXPERIMENTAL RESULTS

The proposed techniques have been implemented in VHDL (Xilinx 9.2) and then the circuits have been synthesized for FPGA VIRTEX-6.. An experimental setup [11] based on the Single Event Upset Simulation Tool (SST) has been used to insert SEUs, the block diagram for which is shown in figure 7. The results obtained are summarized in figure 8,9,10,11 The results clearly indicates the efficiency of the proposed techniques in terms of circuit complexity and area as compared to the traditional approaches[10].

The generic FIR filters have been implemented with 6 and 12 taps using the same structure and coefficient as in [10]. Equations (2) and (3) show the FIR filter coefficients, as mentioned in the references above.

$$h[n] = [-1\ 24\ 50\ 50\ 24\ -1] \quad (2)$$

$$h[n] = [1\ -1\ -9\ 6\ 73\ 120\ 120\ 73\ 6\ -9\ -1\ 1] \quad (3)$$

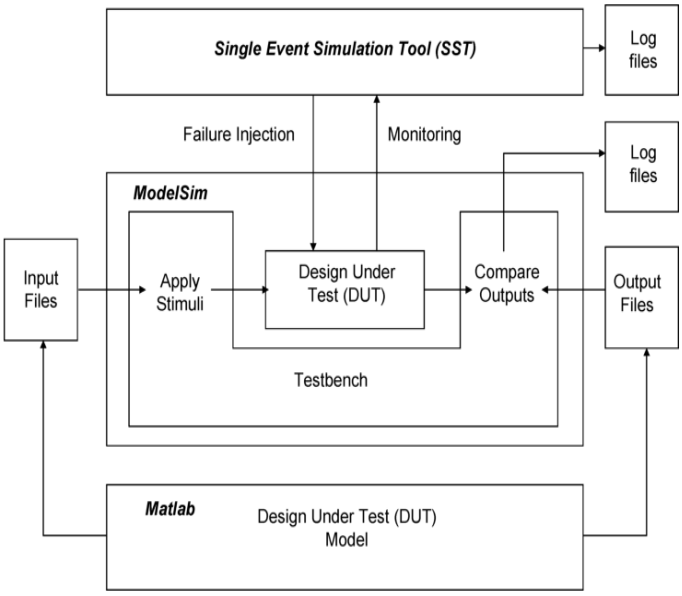

FIGURE 7 : Simulation Environment Block Diagram

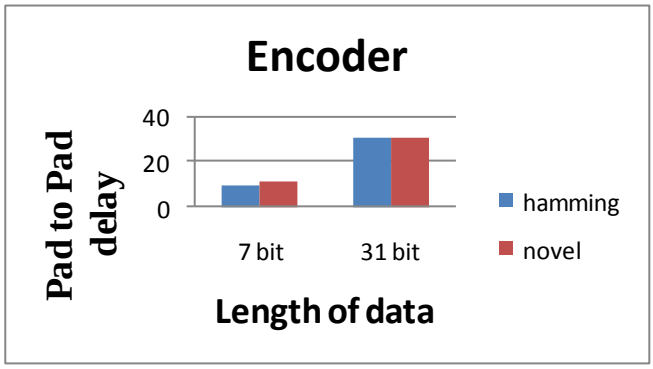

FIGURE 8 : Comparison of Encoders in terms of delay

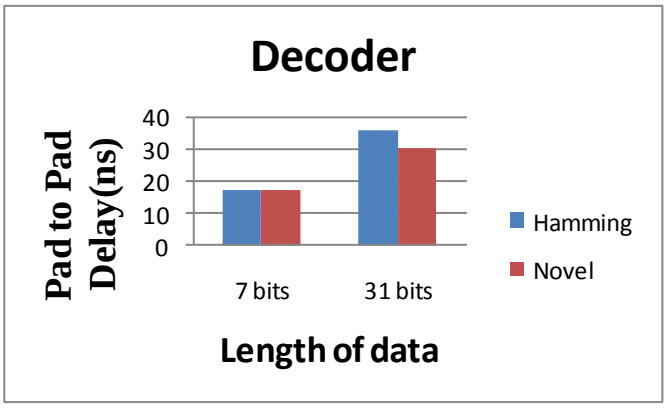

FIGURE 9 : Comparison of Decoders in terms of delay

Table 4 : FPGA Synthesis results for 7 and 31 bits

FPGA - VERTEX 6		FIR FILTER 6 TAPs			FIR FILTER 12 TAPs		
		SLICE	FF	LUT	SLICE	FF	LUT
7 BITS	HAMMING WITH SINGLE ENCODER	42	66	73	69	132	153
	HAMMING ADDITION DATA PROTECTION	27	66	70	61	125	139
	NOVEL HAMMING WITH SINGLE ENCODER	27	66	72	71	132	142
	NOVEL HAMMING ADDITIONAL DATA PROTECTION	31	66	73	61	125	140
31 BITS	HAMMING WITH SINGLE ENCODER	215	254	479	385	476	922
	HAMMING ADDITION DATA PROTECTION	147	254	491	293	445	914
	NOVEL HAMMING WITH SINGLE ENCODER	210	254	454	348	476	911
	NOVEL HAMMING ADDITIONAL DATA PROTECTION	141	254	471	266	445	901

The VIRTEX-6 results shows The decrement in the usage of LUTs when comparing the proposed technique to the ordinary [10] as we increase the no. of bits

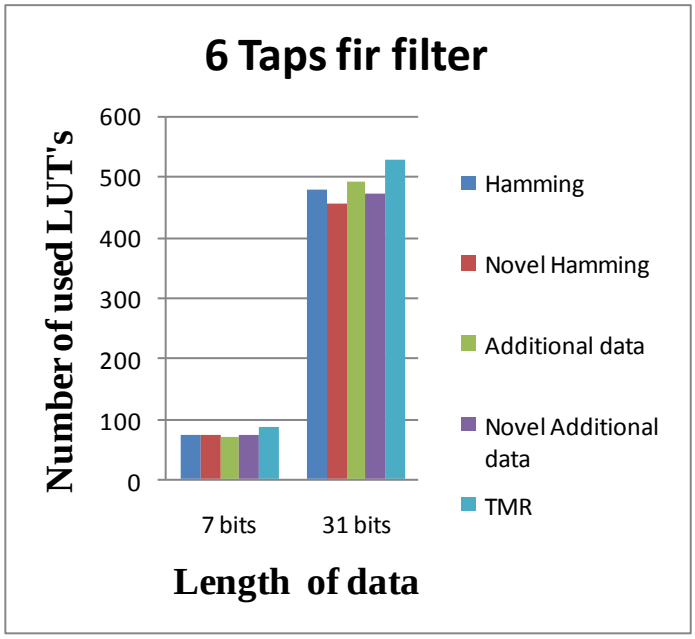

FIGURE 10 : Number of LUTs used in different data protection technique for 6 taps FIR Filter

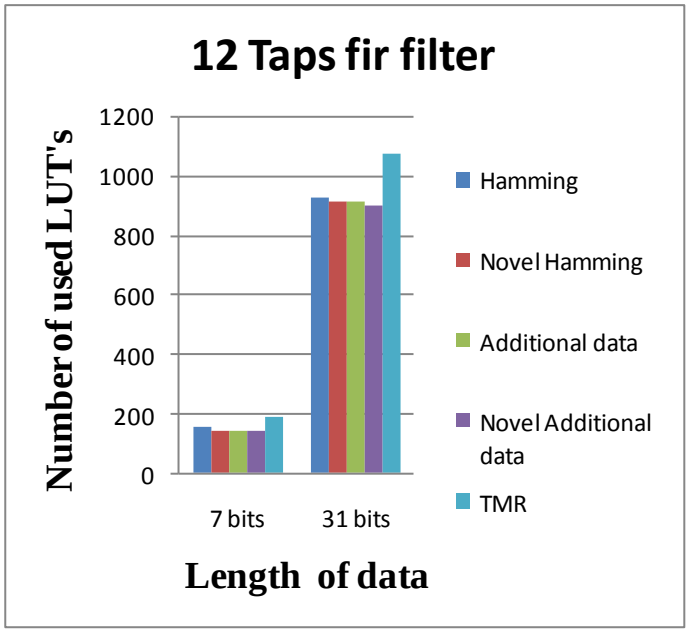

FIGURE 11 : Number of LUTs used in different data protection tech-

nique for 12 taps FIR Filter

5. CONCLUSIONS

In the proposed improvement the redundancy bits are appended at the end of data bits. This eliminates the overhead of interspersing the redundancy bits at the sender end and their removal at the receiver end after checking for single-bit error and consequent correction, if any. Further the effort needed in identifying the values of the redundancy bits is lower in the proposed novel method. Hamming code is normally used for transmission of 7-bit data item. Scaling it for larger data lengths results in a lot of overhead due to interspersing the redundancy bits and their removal later. In contrast, the proposed method is highly scalable without such overhead. We see that there is only 7 bit overhead for a 56-bit data stream, which is much less compared to 4 bit overhead for a 7-bit data**.** A new approach for protecting the FIR filters from single event upsets (SEUs) are implemented in the design. We have focused on achieving low complexity and low area occupancy with minimum delay. Improved method can be scaled easily for larger data lengths as compared to [10]. The simulation results of the proposed designs are encouraging in terms of delay and area used. The implementation results show that the proposed design is suitable to protect FIR filters efficiently from single event upsets. Future work includes the consideration of power consumption as a metric for optimization, since it is a key factor in space applications.

6. REFERENCES

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